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FPGA Benchmarking

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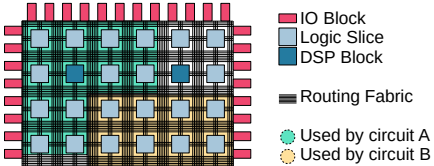
Introduction

- Antwerp Space
  - Founded in 1962 as part of Bell Telephone
  - Since 2010 part of the European OHB group
  - Primarily satellite communications
    - Ground stations
    - On-craft modules
  - Also scientific modules

FPGAs

- What is an FPGA
  - *Field-Programmable Gate Array*
  - Programmable network of digital logic
  - Fast thanks to parallelization
  - Basically equivalent to a custom chip
- Why use an FPGA
  - Price
  - Flexibility
    - Design adjustable once deployed
    - Replacing a chip in orbit is difficult
  - Ideal for DSP at high speed with low latency



Space Hardware

- Low volume
- Long term projects
- Every watt counts
- Radiation!
  - Limits component choice
    - e.g. Xilinx: only Virtex-5QV and Virtex-4QV
  - Very expensive
    - Virtex-5QV 85k€

Component Choice

- Large differences between architectures
  - Pin counts
  - Specialized hardware blocks
  - Internal structure
- Specifications
  - Every manufacturer (or even architecture) uses different metrics
  - Difficult to compare
  - Dubious to rely on
- Software!
  - Just as important as the hardware itself
  - If the software can't synthesize a design, it can't be used

The question: How do you pick an FPGA for a project?
Our answer: Based on hard data: Benchmarking.

Benchmarking

- Determining performance of an FPGA, in this context:
  - Maximal frequency
  - Maximal occupancy rate
- Stamping
  - Filling the FPGA with identical copies of 1 (small) circuit
  - When the software fails: found max occupancy
  - Use the maximal frequency here
  - Repeat for a number of other circuits
- Synthetic results
  - Not a realistic data point
  - Heavily dependent on circuit used
  - Liked, but steerable, by manufacturers

Better Benchmarking

- We want an accurate early estimation of FPGA resources.
- Manufacturer independent
- Very flexible
  - Allow custom parameters and options
- Basic circuits
  - The end user should pick relevant circuit
- Allow background filler
- Requires custom software
  - Automatic creation of datasets

Background Filler

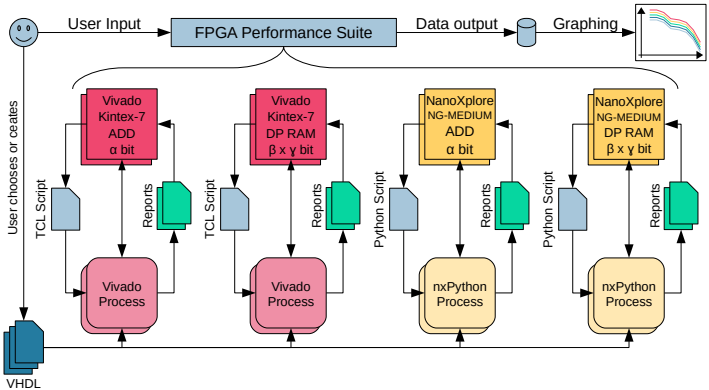
- Simulate routing congestion
- Keep specialized hardware free for actual circuit
- Fill a lot of LUTs with nonsense
- Must be in the data path!
  - Synthesis software is smart
  - Segregates unconnected parts of a design
- Must not be slower than the “real” circuit
- ISCAS’89 Benchmarks
  - Basic combinatorial logic
  - Varied designs, from 13 to 23815 gates

Limitations

- Limited devices for testing
  - Xilinx
    - Vivado
    - Large Kintex-7 part (XC7K410T)
    - 28nm
    - 254 200 LUTs
  - NanoXplore
    - nxMap/nxPython
    - Small part (NG-MEDIUM)
    - 65nm
    - 34 272 LUTs
- Small set of designs
- Limited sets of parameters
  - Mainly to keep computation time reasonable

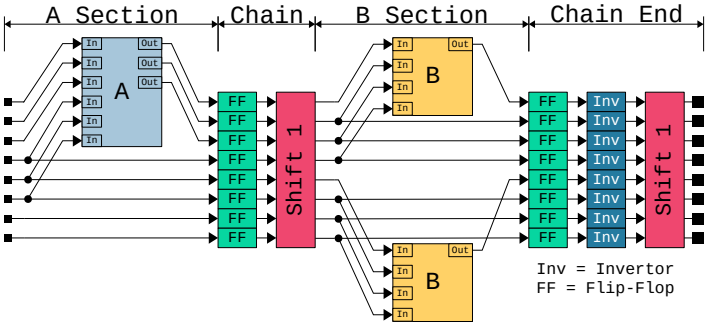
Software Implementation

- User supplies VHDL files
- User sets parameters
- Software automatically runs vendor software
- Parallelized



Background Filler Top Module

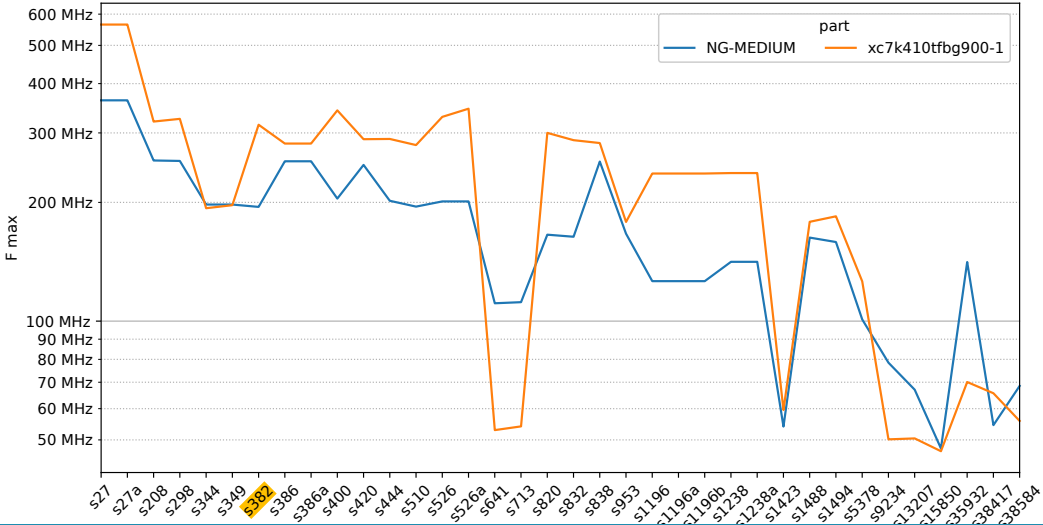
- Chain multiple circuits
- As generic as possible
  - Limited by VHDL
- Keep shifting data path
  - Defeat optimizations



FIR With Background Filler

- Symmetric FIR filter design provided by Antwerp Space
  - Treated as black box
  - 129 tabs, 16 bit data and coefficients
  - 2.7% fill rate
- ISCAS s382 as background filler
  - 0.1% fill rate (easy to calculate with)
  - Faster than base FIR speed ($>$ 200MHz)
- From 1$\times$FIR + 10$\times$Filler to 30$\times$FIR + 500$\times$Filler
  - Only ran if predicted fill rate $<$90%
- Took about a week of night-time running on 28 cores with 128GB RAM
- Due to technical problems, only on Kintex part.

Results ISCAS'89



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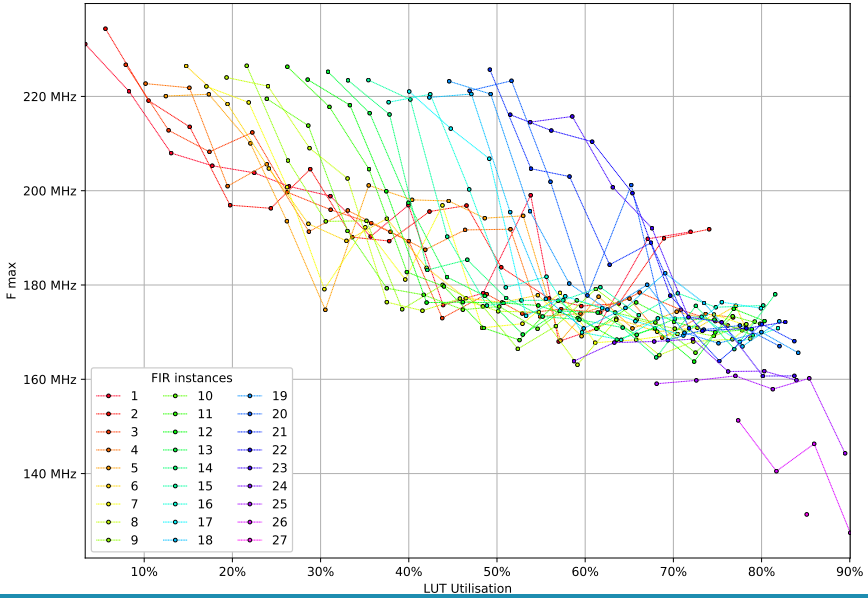
F max
220 MHz
200 MHz
180 MHz
160 MHz
140 MHz
10%
20%
30%
40%
50%
60%
70%
80%
90%
LUT Utilisation
FIR instances
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Conclusion

- Our methodology is more accurate than estimation based on manufacturer data
- Our custom software automates data creation
  - Interpretation still relies on expertise
- Benchmarking and performance estimation is complex

Questions

Thank you for your attention.
Question time!